A Dynamical Load-Cycle Charge Model for RF Power FETs

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***Abstract*—A nonlinear charge model for RF power FETs is presented. The model, intended for use in harmonic-balance simulators, calculates the time evolution of the nonlinear charge in a period of the steady-state regime. For that, the experimentally extracted capacitances are integrated using the device dynamic load cycle as integration path. The proposed approach is technology independent and it has been applied here to a Si LDMOSFET and a SiC MESFET. Load pull measurements have been performed to verify the validity of the model.**

***Index Terms*—Charge model, nonlinear modeling, power FETs.**

I. Introduction

CONVENTIONAL FET technologies based on Silicon or GaAs substrates (GaAs MESFET, GaAs/AlGaAs HEMTs, Si LDMOSFET...) have widely-proven suitability for high-power amplification at different frequency bands [1], [2]. The output power performances of these devices are often limited by their breakdown voltage and thermal conductivity characteristics. Nevertheless, the recent advances on wide bandgap semiconductor materials are pushing forward the boundaries for solid-state RF high power amplification. MESFETs fabricated from 4H-SiC and HFETs fabricated from the AlGaN/GaN heterostructure are the most promising devices to achieve the output power requirements of modern transmitters for wireless applications [3].

Suitable nonlinear models for RF power applications require an accurate representation of both conduction and displacement currents covering the entire device operating regions. The measured intrinsic capacitances of FETs are, commonly nonlinear functions of two control voltages, presenting their largest variations in the ohmic region [4]. Thus, an accurate model, intended for simulation of nonlinear regimes, must take into account the complete dual voltage dependence of the intrinsic capacitances. As an example, recent works that make use of complex expressions for nonlinear charge have shown excellent results in predicting large signal performances of PHEMTs [5]. However, electrical models for microwave power devices have to be constantly revisited due to the rapid evolution of new technologies.

In this work, a FET charge model independent of the device technology is presented. The model is intended for use in harmonic-balance (HB) simulators. The nonlinear charge evolution is obtained from the experimentally extracted intrinsic capacitances by using, as integration path, the dynamic load cycle corresponding to the actual steady-state operation of the device. Unlike [6], it has no constraint on the shape of the dynamic load cycle. Besides, the charge model proposed here does not require explicit expressions for charges (which are generally oriented to a particular technology), avoiding in this way any parameter-fitting procedure. It has been applied to a Si LDMOSFET and to a SiC MESFET.

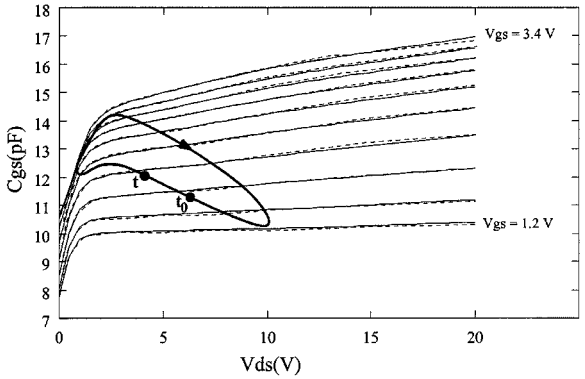

Fig. 1. $C_{\rm gs}$ of the LDMOS transistor as a function of $v_{\rm gs}$ and $v_{\rm ds}$. Dashed line: extracted from multibias S-parameter measurements. Solid line: look-up table model. A generic trajectory in a period of the steady state is superimposed.

II. Charge Model

First, the bias dependence of the device intrinsic capacitances is experimentally obtained. For that, the selection of a particular topology and extraction procedure is required. Here, a classical field effect topology is used, with three nonlinear capacitances, $C_{\rm gs}, C_{\rm gd}$, and $C_{\rm ds}$, and a transconductance time delay τ. Nevertheless, the proposed charge model can be applicable to any other topology. As an example, Fig. 1 shows the dual bias dependence of the gate source capacitance $C_{\rm gs}$ for the LDMOS transistor. This capacitance, together with $C_{\rm gd}$ and $C_{\rm ds}$, is extracted through conventional methods from multi-bias pulsed S-parameters measurements [4], [7]. Assuming a quasistatic approach, the curves shown in Fig. 1 represent the nonlinear dependence of $C_{\rm gs}$ on the two control voltages, $v_{\rm gs}$ and $v_{\rm ds}$. A look-up table model based on piece-wise cubic B-splines [8] is proposed to approximate the voltage dependence of $C_{\rm gs}$. The use of a look-up table model provides an accurate representation of the capacitance (Fig. 1), while keeping the approach technology independent. Similar procedure is applied to $C_{\rm ds}$ and $C_{\rm gd}$, which are also functions of the two control voltages.

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A common way to obtain, in harmonic-balance (HB) simulators, the nonlinear displacement current $i(t)$ associated to a nonlinear capacitance ($C_{\rm gs}$ for instance) function of two variables, is given by [9]

$$i_{C_{\rm gs}}(t) = C_{\rm gs}(v_{\rm gs}, v_{\rm ds})\frac{dv_{\rm gs}(t)}{dt}. \tag{1}$$

However, the average value of this displacement current over a signal period, i.e., the dc current flowing through the two-variable capacitance, can be different from zero [10]

$$\left\langle i_{C_{\rm gs}}(t)\right\rangle = \left\langle C_{\rm gs}(v_{\rm gs}, v_{\rm ds})\frac{dv_{\rm gs}(t)}{dt}\right\rangle \neq 0. \tag{2}$$

This problem is overcome in HB if the frequency-domain displacement current $I_{C_{\rm gs}}(\omega)$ is calculated from $j\omega \cdot Q_{\rm gs}(\omega)$, with $Q_{\rm gs}(\omega)$ being the Fourier transform of the charge variations $q_{\rm gs}(t)$, in a period T of the steady state, associated to the nonlinear capacitance $C_{\rm gs}$.

$$q_{\rm gs}(t) \overset{\text{Fourier}}{\longrightarrow} Q_{\rm gs}(\omega) \overset{j\omega\cdot Q(\omega)}{\longrightarrow} I_{C_{\rm gs}}(\omega)$$

Thus, the key point is to obtain the time variations of the charge associated to each nonlinear capacitance in a period T of the steady state. For that, we suggest the use of the time domain part of the HB algorithm to calculate these time variations of charge by integrating the extracted nonlinear capacitances along the dynamical load cycle.

Let us consider a generic trajectory of $C_{\rm gs}$ in a period of the signal steady state (Fig. 1) associated to a particular load-cycle. For a given load-cycle, the drain-to-source voltage $v_{\rm ds}$ is a function of the gate to source voltage $v_{\rm gs}$. Thus, the evolution of $C_{\rm gs}$ along that trajectory is a function of $v_{\rm gs}$ only. Integrating (1) between time t_0 and time t, the charge $q_{\rm gs}(t)$ can be calculated from

$$\begin{aligned}\int_{t_0}^{t} i_{C_{\rm gs}}(\tau)\,d\tau &= \int_{q_{\rm gs}(t_0)}^{q_{\rm gs}(t)} dq_{\rm gs} \\ &= \int_{v_{\rm gs}(t_0)}^{v_{\rm gs}(t)} C_{\rm gs}(v_{\rm gs}, v_{\rm ds}(v_{\rm gs}))\,dv_{\rm gs} \\ \Rightarrow q_{\rm gs}(t) &= q_{\rm gs}(t_0) + \int_{v_{\rm gs}(t_0)}^{v_{\rm gs}(t)} C_{\rm gs}(v_{\rm gs}, v_{\rm ds}(v_{\rm gs}))\,dv_{\rm gs}.\end{aligned} \tag{3}$$

From (3), it can be seen that the time-domain gate-source charge $q_{\rm gs}(t)$ is obtained by summing up the elemental charges brought by the displacement current during each time slot. Thus, it can be solved in the time domain part of the HB simulation. If a trapezoidal approximation is used, the charge at time-iteration n can be calculated from the capacitance and voltage at time-iteration n and the charge, capacitance, and voltage at time-iteration n$-$1:

$$\begin{aligned}q_{\rm gs}(n) = q_{\rm gs}(n-1) &+ \frac{1}{2}[C_{\rm gs}(n) + C_{\rm gs}(n-1)] \\ &\times [V_{\rm gs}(n) - V_{\rm gs}(n-1)].\end{aligned} \tag{4}$$

The initial value for charge $q_{\rm gs}(0)$ is set arbitrarily to zero since the average value of the charge in a period T has no influence in a harmonic balance analysis. The calculation of $q_{\rm gs}(t)$ is automatically performed by the simulator, at each HB iteration. Obviously, when convergence to the final steady state is reached for the last HB iteration, the integration path corresponds to the actual dynamical load-cycle. Similar procedure is applied to obtain the nonlinear charge variations associated to $C_{\rm gd}(v_{\rm gs}, v_{\rm ds})$ and $C_{\rm ds}(v_{\rm gs}, v_{\rm ds})$. Since the time evolution of the nonlinear charges in a period of the steady state is automatically computed from the extracted intrinsic capacitances at each HB iteration, the modeling procedure does not require explicit expressions of the nonlinear charges versus $v_{\rm ds}$ and $v_{\rm gs}$.

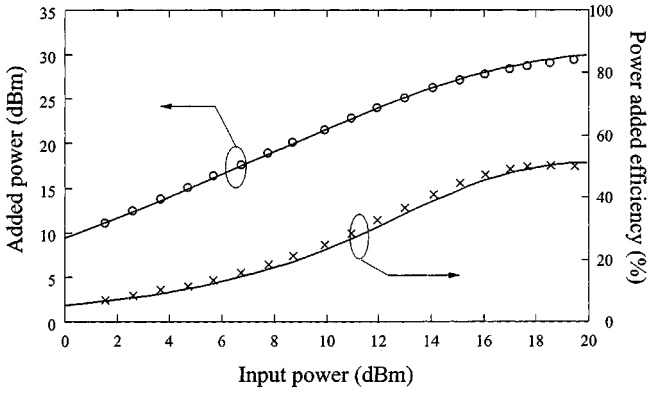

Fig. 2. Added power (PA) and power-added efficiency (PAE) of the LDMOS transistor at 1 GHz. B class ($V_{\rm ds0} = 6$ V, $I_{\rm ds0} = 10$ mA). Circles and crosses: load-pull measurements. Solid line: harmonic-balance simulation.

III. Experimental Results

The proposed charge model has been applied here to two different devices for RF power and medium-power applications: A 1 μm, 21 mm Si LDMOSFET and a 1.2 μm, 250 μm SiC MESFET. Classical field effect topologies together with well-known extraction techniques for extrinsic and intrinsic elements were used in both cases [7]. The nonlinear drain current was described by the look-up table model developed in [8]. The three intrinsic capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are considered as functions of the two control voltages. Active load-pull measurements were carried out to validate the proposed charge model. The load terminations of the active load-pull setup at the harmonic frequencies were measured. The same loads were used during simulation for sake of consistency. Fig. 2 shows the measured and simulated added power, PA, and power added efficiency, PAE, versus input power, for the LDMOS device operating in a B class at 1 GHz. A similar comparison is shown in Fig. 3 for the SiC MESFET operating in an AB class at 1.8 GHz. Good agreement between model predictions and experimental data is obtained in both cases. It is important to notice from Figs. 2 and 3 that the nonlinear model accurately simulates the small-signal regime (very low input power).

Additional comparisons, for different operating conditions, were performed, obtaining similar agreement between measurements and simulations. Moreover, other simulations using a simplified capacitance model (fixed values for $C_{\rm gd}$ and $C_{\rm ds}$ corresponding to the bias point, $C_{\rm gs}$ function of $v_{\rm gs}$ voltage only) were carried out. As found previously by Miller et al. [11], the largest discrepancies were found in the second and third harmonic output powers, and in the device input impedance at

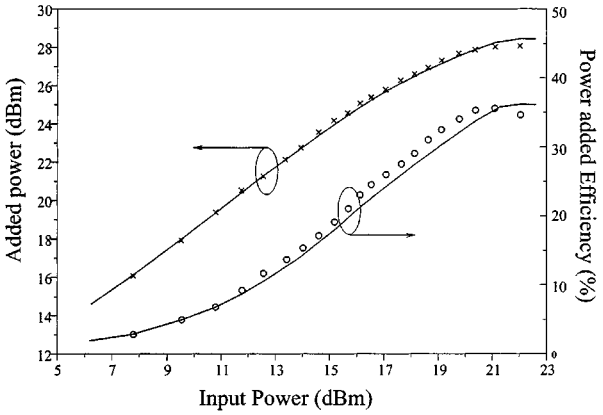

Fig. 3. Added power (PA) and power-added efficiency (PAE) of the SiC MESFET at 1 GHz. AB class ($V_{ds0} = 20$ V, $I_{ds0} = 80$ mA). Circles and crosses: load-pull measurements. Solid line: harmonic-balance simulation.

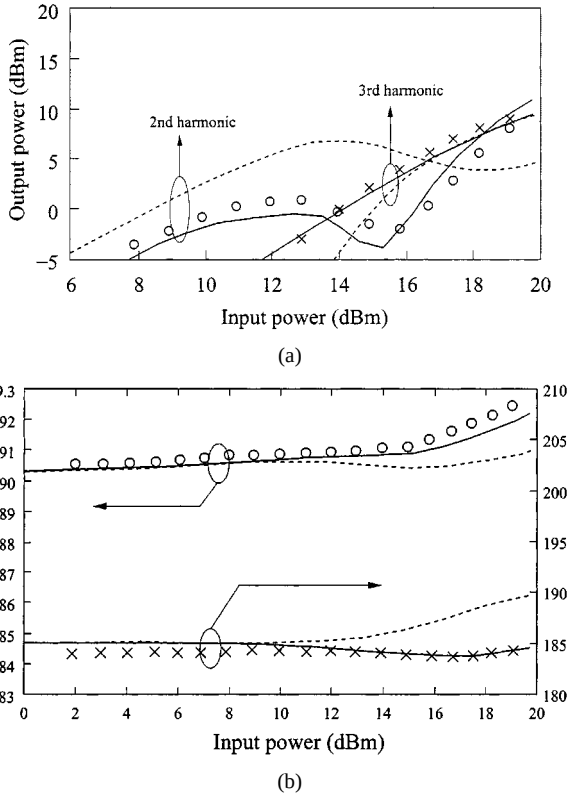

Fig. 4. (a) Second and third harmonic output power of the LDMOS transistor at 1 GHz. (b) Input reflection coefficient of the LDMOS transistor at 1 GHz. Circles and crosses: obtained from load-pull measurements. Dashed line: HB simulation with simplified capacitance model. Solid line: HB simulation with load-cycle charge model.

high compression regime. As an example, Fig. 4(a) shows the output power at second and third harmonics versus input power predicted by both the dynamical load-cycle charge model, and the simplified capacitance model, for the case of the LDMOSFET. The evolution of the LDMOSFET input reflection coefficient versus input power, provided by the two mentioned models, is shown in Fig. 4(b). In both cases, measurements are superimposed, confirming the better accuracy of the dynamic load-cycle charge model at large-signal regimes.

IV. Conclusion

A nonlinear charge model for RF power FETs has been presented. The model, intended for use in harmonic balance simulators, is based on the determination of the time evolution of charge in a period of the steady-state regime. For that, the intrinsic capacitances are integrated using the device dynamic load cycle corresponding to the actual steady state as integration path. The resulting nonlinear charge model is consistent with the small signal model for low power regimes. The modeling approach has been successfully applied to two different technologies for RF power amplification. The good agreement found between simulations and load-pull measurements, from low to high power levels, confirmed the validity of the proposed model. The model procedure is easy and straight, since it only makes use of the experimentally extracted intrinsic capacitances and no explicit expressions of charge versus control voltages are required. Besides, its technology-independent nature makes it particularly suitable for technologies that are constantly under development.

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